DIVISION CIRCUIT USING REVERSIBLE LOGIC GATES

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Abstract— In the recent years, reversible approachis becoming widely used in many domains, such as quantum computing, optical computing and ultra-low power VLSI circuit. Division has its application in the design of reversible Arithmetic Logic Unit (ALU). In this paper, we have exhibited a novel design of division sequential circuit using reversible logic gates. The proposed design of division block is based on reversible gates with reduction of garbage outputs, constant inputs, quantum cost and hardware complexity. The comparative results demonstrate that the proposed solution have less performanceand significantly better scalability than the currentdesigns

Keywords— Low power; reversible ALU; reversible gates; quantum cost; garbage outputs; hardware complexity; constant inputs; reversible division

I. INTRODUCTION

Power consumption is an essential issue in modern day VLSI (Very-Large-Scale Integration) designs. Consumption has become the essential limit of the increasing number of transistors per chip. In the recent years, many techniques have been developed at various levels in CMOS VLSI design.

- At system level and algorithmic level, techniques such as use of dynamic voltage Scaling (DVS) [1] and dynamic power management (DPM), as well as alternate encoding methods.[2].
- At architecture level, techniques such as use of parallel structures, pipelining [3], the clock gating [4].
- At circuit level, techniques such as use of the glitch [5].
- At the technology level, techniques [6] such as VT reduction, multi-threshold voltages have beenused.

Front of these diversity methods that are dedicated to improving the power VLSI design. In this paper we have encountered the reversible logic method [7]. It has wide applications in several technologies such as the nanotechnology, low power CMOS, optical information processing, bio information and DNA computing. In 1961 Rolf Landauer [8] showed that the irreversible logic gatesor the conventional logic gates, set-to-one like AND, OR, XOR and others dissipate a certain amount of energy caused the loss for each bit information during computation (at least kTln2 for each bit of information lost, where K is the Boltzmann's constant and T is the operating temperature).

In 1973, Bennett showed that [9] in order to avoid KT*ln2 joules of energy dissipation in a irreversible circuit, it must be built using reversible logic gates only, since there is no information loss happens in reversible circuits. In fact, division module is very important in the digital processing. Division process is one of the most difficult operations in the ALU and plays a big role in digital signal processing systems. This paper focuses on the design of division circuit sequential using reversible logic gates for

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positiveintegers.

II. BACKGROUND

In this section, we have exhibited the essential principles definitions to reversible logic along with the analysis of quantum cost.

A. ReversibleFunctions

Reversible function can be realized by reversible logic, is a bijection. Then there is a unique one-to-one mapping between an n-input vector and a corresponding n-output vector. Avoid leading output signals of gates to more than one input (Fan_out).Agatewithkinputsandkoutputsiscalled k*k

gate. An k*k reversible logic gate can be denoted as —

, where, = (, ,…,) is the input vector and =(, ,

…,) is the output vector as show in fig.1 [10]. Reversible logic circuits have theoretically zero internal power dissipation because they do not lose data.

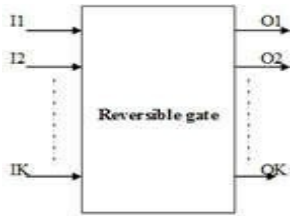

Fig.1. Reversible logic gate

B. Garbageoutputs

That defines the outputs of the reversible gate that is not used for further computations [11] [12]. The unutilized outputs from a gate are called ”garbage output” as show infig.2.

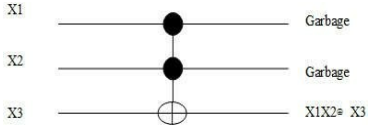

Fig.2. Garbage output

C. Constant inputs

Constant inputs (CIs) refer to the inputs which are used as control inputs and connected to logical '0' or '1' in order to obtain the logical function.

[13].

D. Quantum Cost

Quantum cost is the number of elementary 1*1 like NOT and 2*2 quantum logic gateslikeControlled

,Controlled and CNOT gates[14] [15] needed to realize the circuit.

E. Hardwarecomplexity

This refers to the total number of the logical calculations in a circuit that is measured by counting the number of AND operations, number of NOT operations and number of EX_OR operations [16]. To compute the hardware complexity of the reversible circuits we assume that:

a = Number of EX-OR gates. þ = Number of ANDgates.

6 = Number of NOTgates.

F.Synthesis of reversiblelogic

The design of reversible circuits significantly differs from the design of classical circuits. A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must generate minimum number of garbage outputs. Equally they must use minimum number of constant inputs[17].

The fundamental rules for efficient reversible logic synthesis are:

☐ Reduction the number of quantum cost, garbage outputs, constant inputs and hardwarecomplexity.

☐ Avoid leading output signals of gates to more than one input (fan_out is notpermitted).

☐ Use a less number of reversible gates as conceivable to attain thegoal.

Various reversible gates have been previously proposed by researchers/designers till now [24-30]. Each gate has a cost associated with it called the quantum cost. The NOT gate is a 1-q-bit gates and it has a quantum cost of zero. The N-bit Controlled-Gate has quantum cost of n-1. The Feynman gate can be operates as a controlled NOT (CNOT). If A is set to ‘1’ then

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the gate behaves as a Not gate, else a buffer gate. Feynman gate is widely used to surmount the fan-out problem as fan-out is not allowed in the reversible logic. It has a quantum cost of 1. The quantum cost of a Double Feynman gate is 2. The quantum cost of a Toffoli gate, TR gate and Peres gate are 4. Some examples of reversible logic gates are given by Table.1 [16-20]. These reversible gates help researchers/designers to design higher complex computing circuits. In this manuscript, we employ the reversible approach to realize a Division module.

TABLE1. Examples of some reversible logic gates

Gate	*Quantum cost*
Feynman gate	*1*
Not gate	*1*
Tr gate	*4*
Toffoli gate	*5*
Peres gate	*4*
Fredkin gate	*5*
BHA gate	*4*
BHC gate	*5*

IV. Related work

A. Division operation

Essentially, the parameters of the division operation are dividend X and divisor Y as an input, and the quotient Q and remainder R as output, With X= Q*Y+R. For division, we use shift/adder division algorithm. At every step, we Shifted the register A and X (dividend) of 1 bit to the left. If the content of the register S.A is negative, then we add the contents of register A to Y. Else we subtract the contents of register A to

Y. If the result of subtraction/addition is positive (or zero) then, the quotient bit qi = 1. Else the quotient bit qi = 0. This process is repeated ntimes.

B. Components of division circuit

• Input reversible 8 bitMUX

Figure 3 shows the 2 inputs n-bit reversible MUX where Sel itshe select input, and aretwo inputs. If Sel = 0, then $K_0K_1K_2 \ldots\ldots K_7$ $\ldots\ldots W_0 = L_0 L_1 L_2 \ldots\ldots L_7$ or if S =1, then $W_0W_1W_2 \ldots\ldots W_7 =$. This

$W_0W_1W_2$ $K_0K_1K_2$

$L_0L_1L_2 \ldots\ldots L_7$

reversible MUX consists of n the applicable criteria that follow.BHA[16]gateswhichisgeneratengarbageoutputsan d needs 4n quantumcost

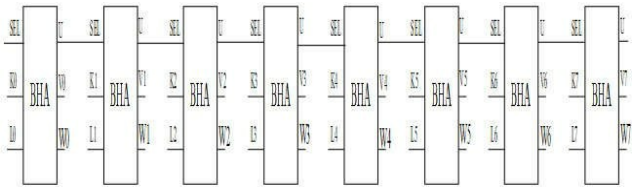

Fig 3. 2-input 8-bit reversible multiplexer circuit

8+1) BIT PARALLEL ADDER/SUBTRACTOR

To perform reversible realization of (n+1) adder/subtractor circuit we may use different combinations of any of the reversible logic gates. In [20] n bit reversible adder/ Subtractor using HNG gates is presented. The carry-out of the adder/ Subtractor is ignored in the proposed division circuit. Then, the implementation of (n+1) bit parallel adder/ subtractor requires n full Adder/Subtractor units and one TS-3 gate as depicted in Fig4.

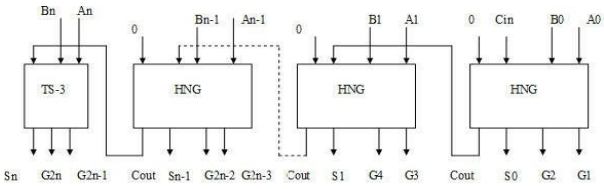

FIG 4. REVERSIBLE (N + 1) BIT PARALLEL ADDER WITH IGNORING OUTPUTCARRY

• N BIT REVERSIBLE PIPO LEFT-SHIFTREGISTERS

In n bit PIPO shift register as show in fig.15, during every clock pulse all information bits are loaded into the register. After shift operation all information bits are transferred together to their respective outputs by the same clock pulse. In [10], an n bits reversible PIPO right- shift register has been proposed. The researchers make it compatible for implementing left-shift

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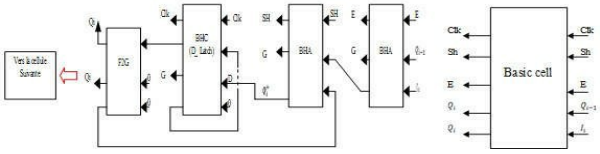
register. Then, the basic elements used to design left shift register are multiplexer and D-latch. Fig 5 shows the proposed left shift register.

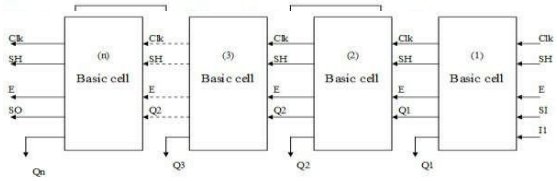
TABLE 2. Function table for reversible PIPO shift register.

SH	E	Finaloutput Q_i^+
0	0	Q_{i-1}(Leftshift)
0	1	I_i(Parallelload)
1		Q_i(Nochange)

Basic cell for 1 bit reversible PIPO(Parallel Input- ParallelOutput)



• 3 to 1 reversibleMUX



• Basic cell for n bit reversible PIPO

Fig 5. Reversible PIPO-left-shift register

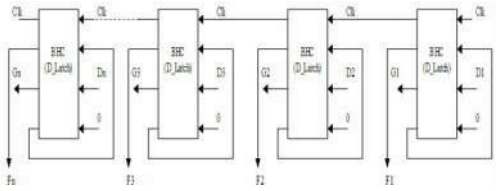
• n- bit reversibleregister

The reversible D-Latch is used in [16] using BHC gate. Then, in order to implement n-bits reversible register we can use n BHC gates. Fig 6 shows the n-bit reversible register. It consists of n BHC gates, produces n garbage outputs, n constant inputs and needs 5n quantum cost. The hardware complexity is 4a+6þ+46.

Fig 6. (n=8)-bit reversible PIPO left shift register

• REVERSIBLE COUNTER (MOD-8)

A mod-8 counter reversible stores an integer



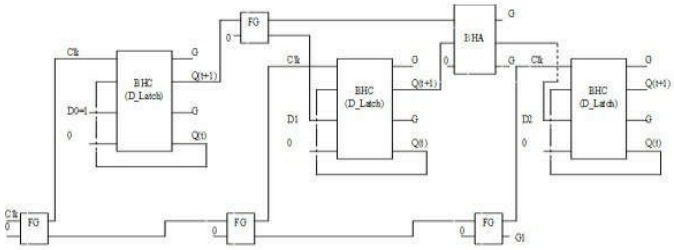
value, and increments that value on each clock tick, and wraps around to 0 if the previous stored value was 7. The BHC gate [16] can be used as a D_ latch,where

So we need three flip-flops D_ latch(BHC)where: =1

=

= .

This reversible circuit produces a total number of 9 garbage outputs and 8 Constant inputs as show in Fig 7. It has a quantum cost of 28.



4 Bit reversiblecomparator

In this section, two 4 bit numbers are compared with each other and the result shows that if one number is superior or fewer than other or if the two numbers are equal with each other. We use NOT gate, TR gate and BJN gate [17]. For example, assume A=A3 A2 A1 A0 and B=B3 B2 B1 B0, for comparing these two numbers, we use these finite state machine as show in Fig8.

Reversible comparator is demonstrated in Fig 9. This circuit produces a total number of 10 constant inputs, 15 garbage outputs, and 18 gates. The quantum cost of this comparator is 38.

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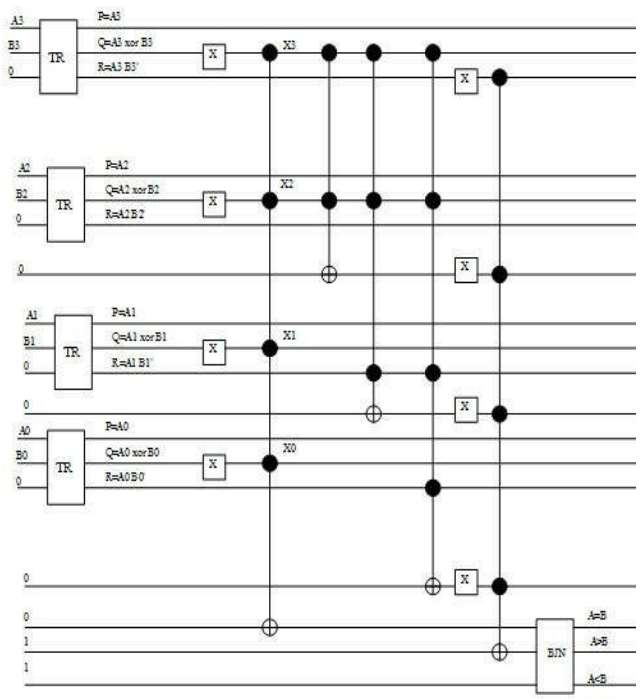


Fig 9. 4 bit reversible comparator.

Reversible n bitdivision

The reversible components are used to implement the division operation. In this paper an optimized reversible non restoring division using reversible logic gates is presented. This circuit includes (n=8).

- ☐ One n bit reversible PIPO left shiftregister
- ☐ One (n+1) bit reversible PIPO left shiftregister
- ☐ One 2 input reversible n bitMUX
- ☐ One 2 input reversible (n+1) bitMUX
- ☐ One (n+1) bit reversible parallel adder/Subtractor. Algorithm:

Inputs:

S.A(…..) = 0 and X(…..) =dividendand Y(…..)=divisor

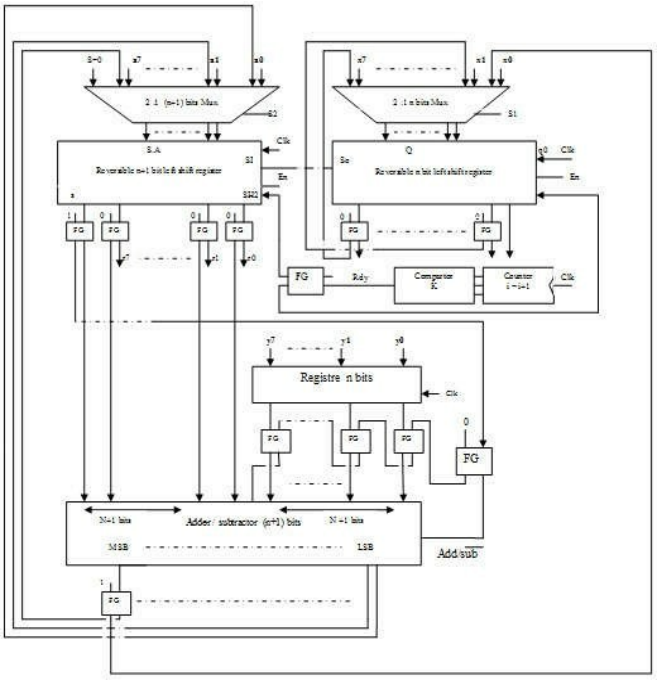
Output

s: Q(…..)=quotientand A(…..)=remainder.

Fig 10. Proposed reversible 8 bit divider circuit

Fig 10 shows the proposed reversible divider circuit. It has 2 PIPO (parallel input-parallel output) left-shift registers. One is n+ 1 bits (n=8) named as S.A and other is n bits named as X. It equally contains an n bits register in order to store the

divisor.Initially ….. =0,X(…..) = dividend, Y (…..) = divisor and rdy = 0. If the division process is completed then, the register X (…..) contains the quotient and S.A (…..) includes the remainder. On the other hand, when S1 = 0 then the two-input n-bit MUXselects dividend X (…..), and if S2 = 0 then the two- input(n+1)bitMUXselects S=0andA(…..)= 0.DuringtheclockpulsewhenE=1,SH1=0andSH2 =0, the output data from n bit MUX and (n+1)-bit MUX are loaded into X and S.A respectively. When E = 0, both S.A and X act as left-shift registers. Initially the value of S is not important, it is important just after the left shift of S.A&X (&=Concatenated), (S.A&X means SO of register X is connected to SI of S.A). If S is high (‘1’) then S.A-Y is performed, else, S.A+Y is computed. The complement of the MSB (most significant bit) is loaded into q0 bit position of register X. In addition, the sum is loaded into register S.A during next clock cycle (S1= 0). It includes 2n+1 clock signals to store the quotient value into register X. Finally, after 2n+1 clock signal, X stores the quotient and A stores the



remainder indefinitely.

D. DIVISION PROCESS EXAMPLE(14/2)

Elementary operation	*S.A3A2A1A0*	*X3X2X1X0*
loading registers	*00000*	*1110*
Shift	*00001*	*110-*
Subtractor	*00001* *11101* *1111*	*1100*
Shift *Adder*	*11111* *000100* *0001*	*100-* *1001*
Shift *Subtractor*	*00011* *11101* *1* *00001*	*001-* *0011*
Shift *Subtractor*	*00010* *11101* *10000* *Final remainder*	*011-* *0111* *Quotient*

Reversible components	*Constant inputs*	*Quantum cost*	*Garbage outputs*	*Hardware Complexity HC(n=1)*
n bit MUX 2 :1	*0*	*4n*	*n*	*2a+ 4þ+36*
(n+1) bit MUX 2 :1	*0*	*4n+4*	*n+1*	*4a+ 8þ+66*
(n)-bit register	*n*	*5n*	*n+1*	*4a+ 6þ+46*
n-bit left shift register	*3n*	*15n*	*3n+2*	*10a+14þ+106*
(n+1)-bit left shift register	*3n+3*	*15n+15*	*3n+5*	*20a+28þ+206*
(n+1)-bit parallel adder/ subtactor	*n*	*6n+2*	*2n+2*	*7a+ 2þ*
Feynman n-bit	*2n+5*	*3n+3*	*0*	*6 a*

reversible MUX: number of garbage outputs

= n, quantum cost = 4n, constant inputs=0 and the hardware complexity 2a+4þ+36.

☐ n+1-bitreversibleMUX:numberofgarbageoutputs = n+1, quantum cost = 4n+4, constant inputs=0 and the hardware complexity 4a+8þ+66.

☐ n-bit register: number of garbage outputs = n+1, quantum cost = 5n, constant inputs=n and the hardware complexity 4a+6þ+46.

☐ n-bit left shift register: number of garbage outputs = 3n+2, quantum cost = 15n, constant inputs=3n and the hardware complexity 10a+14þ+106.

☐ (n+1)-bit left shift register: number of garbage outputs = 3n+5, quantum cost = 15n+15, constant inputs=3n+3 and the hardware complexity 20a+ 28þ+206.

☐ (n+1)-bit parallel adder/ subtactor: number of garbage outputs = 2n+2, quantum cost = 6n+2, constant inputs=n and the hardware complexity 7a+ 2þ.

☐ Other gates (Feynman gate): number of garbage outputs = 0, quantum cost = 3n+3, constant inputs=2n+5 and the hardware complexity 7a+2þ.

VI. COMPARISON

In this section, we have compared the performance of the proposed design with some existing designs as depicted in table 4.

TABLE4.
Comparison

Conception	*Constant inputs(n=8)*	*Quantum cost(n=8)*	*Garbage outputs (n=8)*	*Hardware complexity(n=1)*
This work	*88*	*440*	*99*	*53a + 62þ + 436*
Existing design in [16]	*89*	*454*	*103*	*65a +74 þ+526*
Existing design in [10]	*91*	*538*	*106*	*59a + 67þ + 336*
Existing design in [13]	*103*	*674*	*116*	*84a + 82þ + 426*

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Existing design in [14]	*16 1*	*8 4 6*	*1 8 1*	*91a + 98þ + 506*

Table 4 gives a comparison between the existing and the proposed 8 bits division designs. The proposed design reduces the garbage output, quantum cost, constant inputs as well as the hardwarecomplexity.

VII. CONCLUSION AND FUTUREWORK

In this manuscript, we proposed one approach for designing reversible division circuits. Then we have optimized our design. We have compared this proposed design with the existing designs. The proposed module for non-restoring division has better performance in terms of constant inputs, garbage output, and quantum cost as well as the hardware complexity than that of existing designs. In the future works we will design complete reversible ALU, develop reversible hardware description language and reversible synthesis tools.

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